

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	8	"522298"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/22 06:07
L2	7	"5422298"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/22 06:14
L5	504	(precision adj resistor) same series	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/22 06:17
L6	163	(precision adj resistor) same series with current	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/22 06:17
L7	30	(precision adj resistor) same series with current with resistance	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/22 06:22
L8	447	(resistance resistor) same series with current with (dimension size)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/22 08:29
L9	13	8 and resistor with polysilicon	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/22 06:24
L10	0	(first adj resistor with first adj resistance with target adj resistance with dimension). clm.	US-PGPU B	OR	ON	2005/12/22 08:32
S40	12531	((trench near3 (isolator insolation)) 'locos' 'fox' 'sti') with substrate	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 09:16
S41	1028	S40 and ((trench near3 (isolator insolation)) 'locos' 'fox' 'sti' substrate) with crystalline	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 09:19

S42	662	S41 and ((trench near3 (isolator insolation)) 'locos' 'fox' 'sti' substrate crystalline) with mask\$3	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 09:56
S43	644	S42 and ((trench near3 (isolator insolation)) 'locos' 'fox' 'sti' substrate crystalline mask\$3) with (pattern\$3 etch\$3)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 09:21
S44	2740	S40 and ((trench near3 (isolator insolation)) 'locos' 'fox' 'sti' substrate) with \$6crystalline	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 09:19
S45	1892	S44 and ((trench near3 (isolator insolation)) 'locos' 'fox' 'sti' substrate \$6crystalline) with mask\$3	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 09:20
S46	1834	S45 and ((trench near3 (isolator insolation)) 'locos' 'fox' 'sti' substrate \$6crystalline mask\$3) with (pattern\$3 etch\$3)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 09:20
S47	1792	S46 and surface	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 09:21
S48	1079	S47 and dielectric	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 09:22
S49	1050	S48 and thick\$4	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 09:23
S50	295	S49 and (pillar column\$4)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 09:24
S51	657	S41 and ((trench near3 (isolator insolation)) 'locos' 'fox' 'sti' substrate ((mono single) near2 crystalline)) with mask\$3	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 09:57

S52	657	S51 and (((trench near3 (isolator insolation)) 'locos' 'fox' 'sti' substrate ((mono single) near2 crystalline)) mask\$3) with mask\$3	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 09:58
S53	639	S51 and (((trench near3 (isolator insolation)) 'locos' 'fox' 'sti' substrate ((mono single) near2 crystalline)) mask\$3) with (pattern\$4 etch\$3)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 09:59
S54	163	S53 and (pillar column\$3 stud\$2)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 10:01
S55	146	S54 and memory	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 10:01
S56	61	self adj compensat\$3 with resistor	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 18:22
S57	3026	substrate with (resistor near5 (first second))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 18:24
S58	188	substrate with ((resistor near5 (first second)) with series)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 18:27
S59	19002	((resistor near5 (first second)) with series)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 18:28
S60	2565	S59 and ((resistor near5 (first second)) with series) with resistance	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 18:28
S61	137	S59 and ((resistor near5 (first second)) with series) with (resistance with (sum total))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/21 18:29

S62	99	S61 and ((resistor first second series resistance sum total) with current)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/12/22 06:07
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